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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/729,544
Filing Date: December 05, 2003
Appellant(s): WATTS ET AL.

Nathaniel Levin
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/22/2006 appealing from the Office action mailed 06/16/2006.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

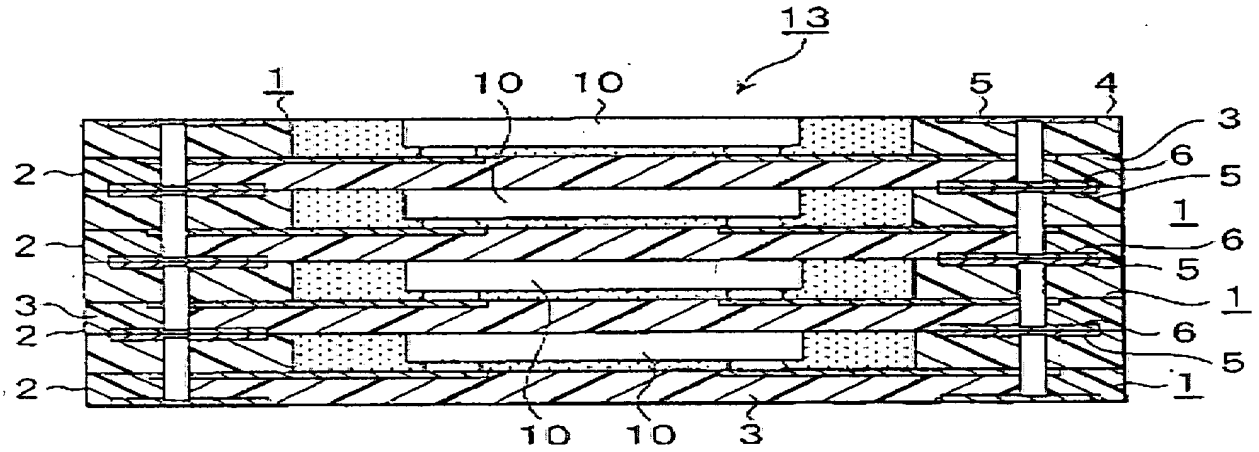
The following ground(s) of rejection are applicable to the appealed claims:

Initially, and with respect to claims 15, 19 and 37, it is note that a "product by process" claim is directed to the product per se, no matter how actually made. See In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which makes it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe, even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. In re Brown, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); In re Pilkington, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); Buono v. Yankee Maid Dress Corp., 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935).

Claims 15, 17, 18, 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murayama et al. (US 6,548,330) in view of in view of Sota (US 6,201,707).

Regarding claims 15 and 34, Murayama (e.g. fig. 6) shows an article of manufacture, comprising: at least two integrated circuit (IC) packages in stacked relation to each other, each of the IC packages including: a substrate an IC 10 mounted on a surface of the substrate 2; a ground plane 6 formed on an opposite surface of the substrate from the first surface on which the IC is mounted; and a coverlay laminated on

the surface of the substrate and having an opening; and at least one conductive connection 8 formed through one of the coverlays and connecting one of the ICs to another of the ICs wherein each IC is positioned in an opening of a respective one of the coverlays.



In regards to the method used to form the opening in the first/second coverlay such as photolithography, it is considered to be an intermediate process step that does not affect the structure of the final device. Although Murayama does not specify which materials can be used for making the substrate and the coverlay, it is well known in the art to use of flexible and thermally stable organic polymers for making IC substrates. In the instant case, Sato discloses that wiring substrates can be made from a variety of materials such as polyimide, polyamide, BT resin, epoxy and polyester. From the viewpoint of costs and ease of machining, it is preferable to use polyimide (col. 5/lls. 24-33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the substrate of Murayama (e.g. layers 2/4) of a flexible and thermally stable organic polymer such as polyimide because it is a preferable material from the viewpoint of costs and ease of machining as taught by Sato.

Regarding claims 17, 18 and 36 Murayama in view of Sato shows that the substrate/coverlay are made of a flexible material such polyimide.

Claims 19, 21, 22, 37 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murayama et al. (US 6,548,330) in view of in view of Sota (US 6,201,707) further in of Blumenau et al. (US 6,421,711).

Regarding claims 19 and 37, Murayama (e.g. fig. 6) shows an apparatus comprising: a stacked integrated circuit (IC) package which includes: a first substrate 1; a first IC 10 mounted on a surface of the first substrate; a first coverlay 4 laminated on the surface of the first substrate and having at least one opening; a second substrate 1 positioned in stacked fashion on the first coverlay; a second IC 10 mounted on a surface of the second substrate; a second coverlay 4 laminated on the surface of the second substrate and having at least one opening; and at least one conductive connection 7/8 connecting the first IC to the second IC and passing through at least one opening in the first coverlay; wherein: the first IC is positioned in an opening in the first coverlay, all of the first IC being in said opening in the first coverlay; and the second IC is positioned in an opening in the second coverlay, all of the second IC being in said opening in the second coverlay. Also, Murayama shows that the first and second substrate include first/second ground planes 6 formed on opposite surfaces of respectively first surfaces on which the ICs are mounted. In regards to claim limitation referring to the process used to make the opening in the first/second coverlay such as photolithography, it is considered to be an intermediate process step that does not affect the structure of the final device. Although Murayama does not specify which materials can be used for

making the substrate and the coverlay, it is well known in the art the use of flexible and thermally stable organic polymers to make IC substrates. In the instant case, Sato discloses that wiring substrates can be made from a variety of materials such as polyimide, polyamide, BT resin, epoxy and polyester. From the viewpoint of costs and ease of machining, it is preferable to use polyimide (col. 5/lls. 24-33). Also, Murayama does not teach a communication device couple to the first IC. Blumenau discloses a communication device such wireless data transceiver is couple to a chip to permit remote interrogation (col. 37/lls. 4-11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the substrate of Murayama (e.g. layers 2/4) of a flexible and thermally stable organic polymer such as polyimide because it is a preferable material from the viewpoint of costs and ease of machining as taught by Sato and to connect a communication device such wireless data transceiver to the first and/or second IC disclosed by Murayama in view of Sato to permit remote interrogation of the chip as taught by Blumenau. Note that the first and second substrates are equivalent.

Regarding claims 21, 22 and 39 Murayama in view of Sato further in view of Blumenau shows that the substrates/coverlays are made of a flexible material such polyimide.

Claims 40 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murayama et al. (US 6,548,330) in view of in view of Sota (US 6,201,707) further in view of Rokugawa et al. (US 6,441,314).

Regarding claims 40 and 42, Murayama in view of Sota does not teach that the a first and second solder mask layers covering the first and second ground planes 6. Nevertheless, Rokugawa teaches a substrate that includes a solder mask 26 covering the ground planes 24. It would have been obvious to one of ordinary skill in the art at the time the invention was made to cover the first and second ground plane with a first and second solder mask respectively as taught by Rokugawa to protect the exposed area of the grounds planes from corrosion.

Claims 41 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murayama et al. (US 6,548,330) in view of in view of Sota (US 6,201,707) further in of Blumenau et al. (US 6,421,711) further in view of Rokugawa et al. (US 6,441,314).

Regarding claims 41 and 43, Murayama in view of Sota further in view of Blumenau does not teach that the a first and second solder mask layers covering the first and second ground planes 6. Nevertheless, Rokugawa teaches a substrate that includes a solder mask 26 covering the ground planes 24. It would have been obvious to one of ordinary skill in the art at the time the invention was made to cover the first and second ground plane with a first and second solder mask respectively as taught by Rokugawa to protect the exposed area of the grounds planes from corrosion.

(10) Response to Argument

Appellant argues that the interpretation given by the examiner to the term "ground plane" is unreasonable and contrary to the plain meaning of the term, as it would be understood by those skilled in the art. However, if a prima facie case of anticipation/obviousness is established, the burden shifts to the applicant to come

forward with arguments and/or evidence to rebut the prima facie case. See, e.g., Dillon, *919 F.2d at 692, 16 USPQ2d at 1901.* Rebuttal evidence and arguments can be presented in the specification, *In re Soni, 54 F.3d 746, 750, 34 USPQ2d 1684, 1687 (Fed. Cir. 1995), by counsel, In re Chu, 66 F.3d 292, 299, 36 USPQ2d 1089, 1094-95 (Fed. Cir. 1995)*, or by way of an affidavit or declaration under 37 CFR 1.132, e.g., Soni, 54 F.3d at 750, 34 USPQ2d at 1687; In re Piasecki, 745 F.2d 1468, 1474, 223 USPQ 785, 789-90 (Fed. Cir. 1984). However, arguments of counsel cannot take the place of factually supported objective evidence. See, e.g., *In re Huang, 100 F.3d 135,139-40, 40 USPQ2d 1685, 1689 (Fed. Cir. 1996); In re De Blauwe, 736 F.2d 699, 705, 222 USPQ 191, 196 (Fed. Cir. 1984).* In this case, appellant did not presented any evidence or factual arguments of why the interconnection layer 6 disclosed by Murayama cannot be recognized as ground plane. It is respectfully noted, that the term "ground plane" does not imply any specific structure or size. Thus the term is considered to be either a functional description or a label. Since pending claims are directed to a structure any intended use and/or other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. *In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).* As it is known in the art, any interconnection layer formed on or within a circuit board is capable of work as ground plane because it can be connected to ground

voltage. Ground voltage is an earth connected electrical conducting connection or the electrical "zero" state, used as the reference voltage in a computer system. Note that specific functionality of the metal layer 6 (ground, power supply, signal) does not further limit the structure. A metal layer is a metal layer regardless to which voltage is connected.

Appellant argues that the size of the metal layer 6 is too small to be characterized as a plane. However, the conductive layer 6 is plane regardless of its size.

Appellant argues that the layer 6 is unsuitable to serve as a ground, since it is not located in the right place and if it were really a ground plane, it would completely fail to perform its intended function of interconnecting the ICs 10. Nonetheless, the fact that some of the interconnections may be commonly connected to ground does not imply that the other interconnections cannot be connected to power or signal voltages. Any operable electronic apparatus must include at least a ground and a power connection.

Appellant agues the modification suggested by Rokugawa would cause the layers 6 disclosed by Murayama to be insulated from below, and therefore unable to perform their intended function of providing a signal connection to a lower level of staked structure. However, in the instant combination the solder masks only cover the exposed areas of the "ground plane" and not the contacting areas as suggested by appellant because only the exposed areas may require environmental protection.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Leonardo Andújar
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Conferees:

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Supervisory Patent Examiner Art Unit 2873

La/LA
March 14, 2007